TEMIC

Siliconix

SUP/SUB75N06-08

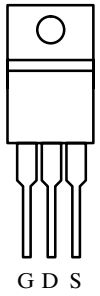
N-Channel Enhancement-Mode Transistors

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.008	75[a]

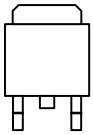
TO-220AB



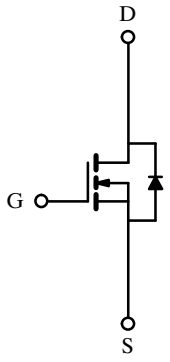
Top View
SUP75N06-08

DRAIN connected to TAB

TO-263



Top View
SUB75N06-08



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	75[a]	A
	T_C = 125°C		55	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Repetitive Avalanche Energy[b]	L = 0.1 mH	E_{AR}	280	mJ
Power Dissipation	T_C = 25°C (TO-220AB and TO-263)	P_D	187[c]	W
	T_A = 25°C (TO-263)[d]		3.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263)[d]	R_{thJA}	40	°C/W
	Free Air (TO-220AB)		62.5	
Junction-to-Case		R_{thJC}	0.8	

Notes
a. Package limited.
b. Duty cycle ≤ 1%.
c. See SOA curve for voltage derating.
d. When mounted on 1" square PCB (FR-4 material).

SUP/SUB75N06-08

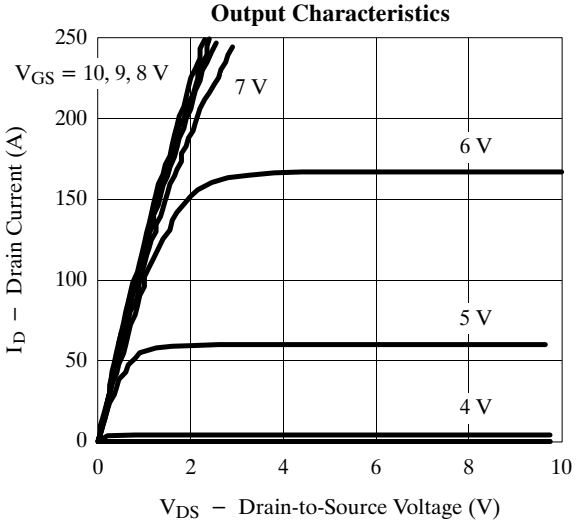
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 125°C			50	
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 175°C			150	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	120			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A		0.007	0.008	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C			0.012	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C			0.016	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	30			S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4800		pF
Output Capacitance	C_{oss}			910		
Reverse Transfer Capacitance	C_{rss}			270		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 75 A		85	120	nC
Gate-Source Charge[c]	Q_{gs}			28		
Gate-Drain Charge[c]	Q_{gd}			26		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.47 Ω I_D ≅ 75 A, V_{GEN} = 10 V, R_G = 2.5 Ω		20	40	ns
Rise Time[c]	t_r			95	200	
Turn-Off Delay Time[c]	$t_{d(off)}$			65	120	
Fall Time[c]	t_f			20	60	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[a]						
Continuous Current	I_S				75	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 75 A , V_{GS} = 0 V		1.0	1.3	V
Reverse Recovery Time	t_{rr}	I_F = 75 A, di/dt = 100 A/µs		67	120	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			6	8	A
Reverse Recovery Charge	Q_{rr}			0.2	0.48	µC

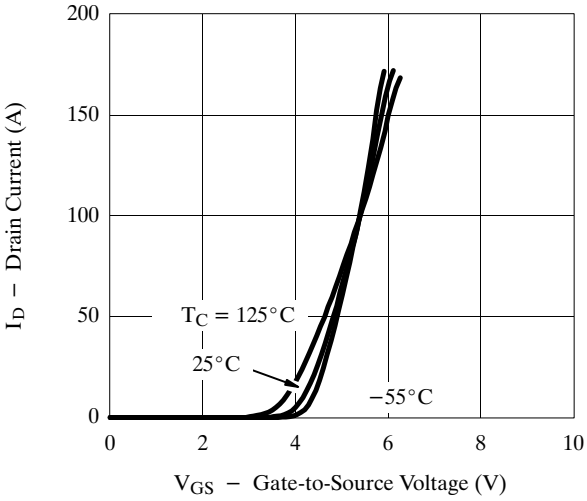
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test: pulse width ≤ 300 µsec, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

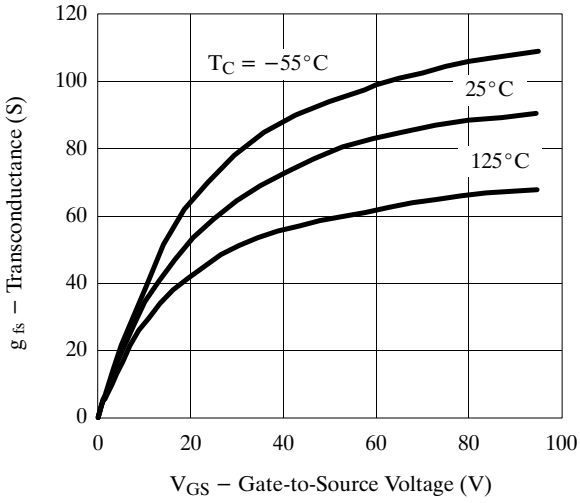
Output Characteristics



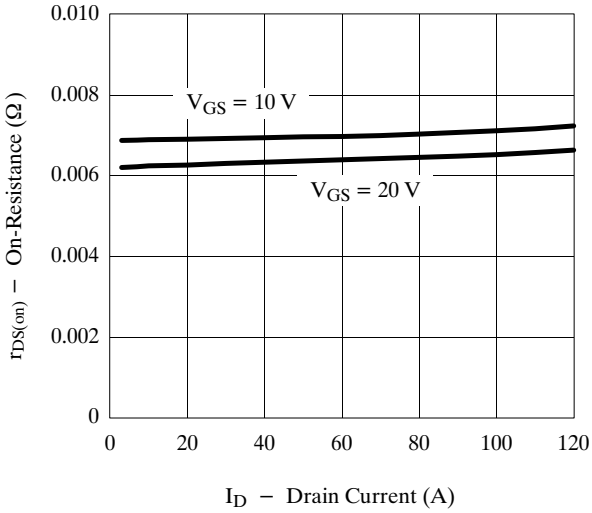
Transfer Characteristics



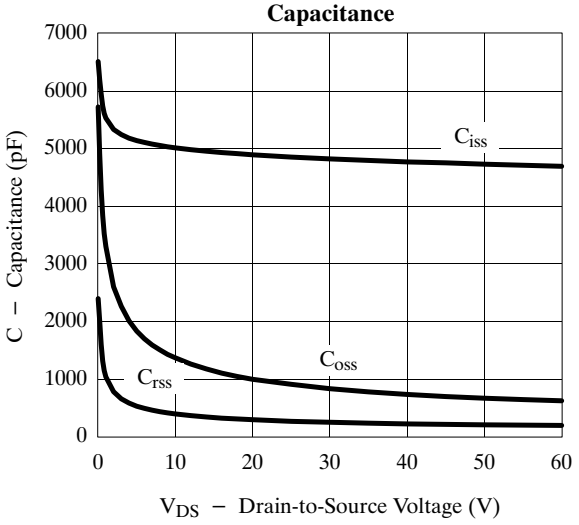
Transconductance



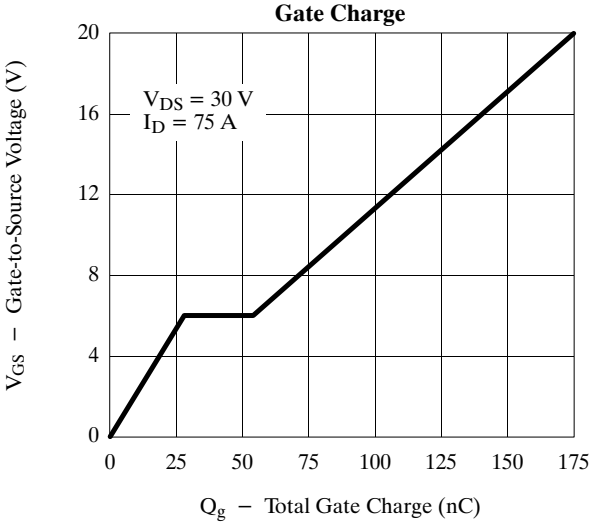
On-Resistance vs. Drain Current



Capacitance



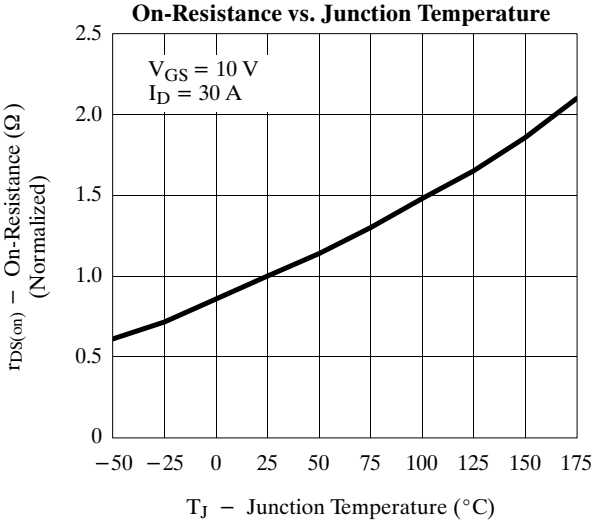
Gate Charge



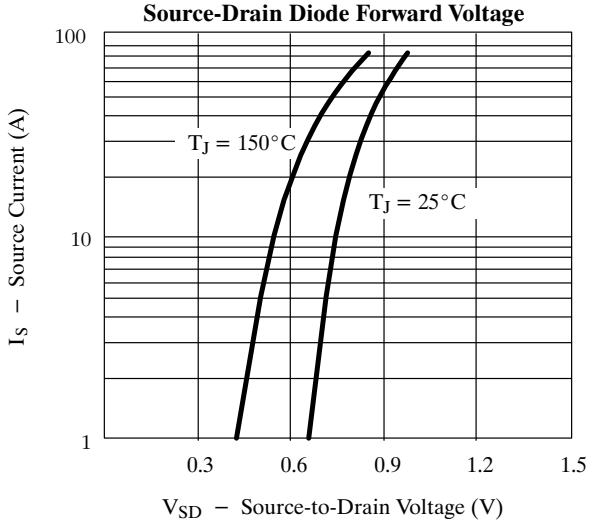
SUP/SUB75N06-08

Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

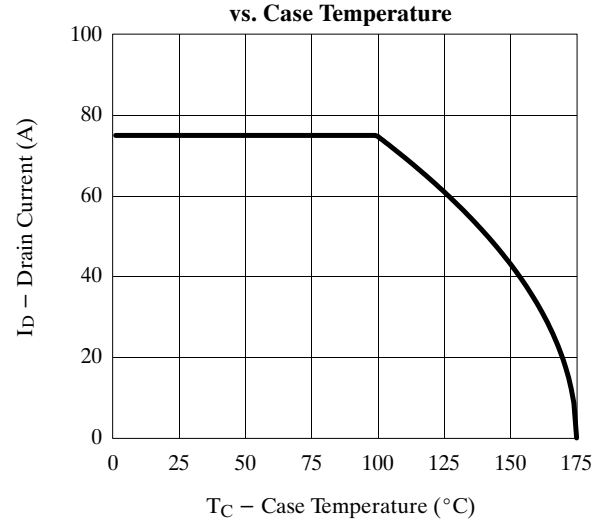


Source-Drain Diode Forward Voltage

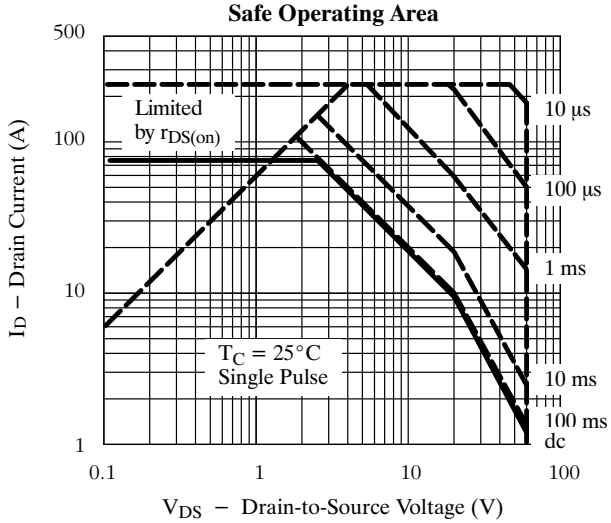


Thermal Ratings

Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case